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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,694	11/11/2002	Laura S. Chadwick	BUR920010195	2341

30449 7590 09/06/2005

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,694	CHADWICK ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 1004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11, 12/ 02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of invention Group I (Claims 1-10) in the reply filed on 7/2/1004 is acknowledged. The traversal is on the grounds that the search and the examination of the entire application could be made without serious burden, since the subject matter of all claims 1-20 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter. This is not found persuasive because the inventions are distinct for the reasons given in the Election/Restrictions Office Action, dated 6/14/2004, and have acquired a separate status in the art because of their recognized divergent subject matter, and therefore restriction for examination purposes as indicated is proper. For example, Group I (Claims 1-10) is drawn to a method of testing a DRAM, which is classified in class 714, subclass 710. The requirement is still deemed proper and is therefore made FINAL.

Claims 11-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7/2/1004.

Specification

The abstract of the disclosure is objected to because it fails to comply with the proper language and format. The abstract should be in narrative form and should avoid using legal 'phraseology, such as comprises, and "wherein" recited through the abstract.

The Examiner is recommending that the opening expression, "A method and system for testing a DRAM comprised of DRAM blocks. The method comprises: in a processor based built-in self test system, generating a test data..." be changed to "A method and system for testing DRAM blocks including, in a processor based built-in self test system, generating a test data..." Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ochi (US 20030128045) Published: July 10, 2003, Filed: June 20, 2002.

Regarding Claim 1, Ochi discloses a method of testing a plurality of semiconductor device under test (DUTs), such as DRAM blocks, each DUT connected to a test circuit, (see, Abstract and Figures 1 and 2), comprising:

Generating a test pattern using a test pattern generator (ALPG 1), where the test pattern output is coupled to a driver circuit (21A, B...N), which produces a test signal corresponding to (DUTs 1, 2...N).

Performing a write operation by sending a write signal into each DUT (DUTs 1, 2...N) through a corresponding driver circuit (21A, B ...N) in response to a test pattern output from the test pattern generator.

Performing a pause for a predetermined period of time, using a timer (24A, B ..N) for setting a pause time and read time of each DUT and then performing a read operation by reading the resulting pattern from each DUT through a corresponding comparator (23A, B ...N) which compares the read signal with a predetermined reference value (not shown) and determines the DUT is defective or acceptable.

The write operation is performed before the pause and the read operation is performed after the pause for the predetermined period of time, in Figure 2, which is a diagram showing the procedures for simultaneously subjecting to a pause test two DUTs. The pausing (t1-t2) of DUT 1 overlaps in time with the pausing (t1-t4) of DUT 2.

Regarding Claims 2, 4, Ochi provides a test apparatus and method, which enable simultaneous testing of a plurality of memory devices, the memory devices providing different levels of performance, particularly, different levels of pausing capability, (see,

Abstract and Summary of the Invention). Also, see Figure 2, which is a diagram showing the procedures for simultaneously subjecting to a pause test two DUTs.

Regarding Claims 3, 6, Ochi discloses enabling simultaneous testing of a plurality of memory devices by performing a simultaneous write operation for each DUT (DUTs 1, 2...N) through a corresponding driver circuit (21A, B ...N) in response to a test pattern output from the test pattern generator, and then performing a simultaneous read operation by reading the resulting pattern from each DUT through a corresponding comparator (23A, B ...N) which compares the read signal with a predetermined reference value (not shown) and determines the DUT is defective or acceptable. With respect to claimed feature of "performing a write and a read operation **sequentially** from a first DRAM block to a last DRAM block of the multiplicity of DRAM blocks", Ochi recognizes that one may perform **sequential write or read on one** DRAM block at a time of plurality of memory devices, by describing a related-art tester for measuring memory devices of different capabilities on a one-by-one basis. However, measurement of memory devices on a per-device basis involves consumption of a very long measurement time. This results in a drop in processing capability, which in turn leads to a hike in testing costs, (see, Background Art).

Regarding Claim 5, Ochi discloses the total writing operation time (t0-t2) of DUT 1 and DUT 2 overlaps in time with (t0-t5), where pausing (t1-t4) overlaps with (t0-t5), see Figure 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochi (US 20030128045) in view of Schwarz (U.S. Patent No. 6,496,947) FILED: October 25, 1999.

Regarding Claims 7-9, Ochi substantially discloses the claimed invention as described in claim 1, including comparators (23A, B ...N) for each DUT, which compare the read signal with a predetermined reference value (not shown) and determine the corresponding DUT is defective or acceptable.

Ochi does not explicitly disclose, "determining redundancy allocation information based on said resulting data pattern; and storing said redundancy allocation information for each said DRAM in separate registers, the storing of any previous redundancy allocation information for a previous DRAM block of said multiplicity of DRAM blocks being completed before the storing of subsequent redundancy information for a subsequent DRAM block of said multiplicity of said DRAM blocks, wherein the number of the registers is equal to the number of said DRAM blocks, and wherein the registers are coupled in series and further including scanning out each **register sequentially".**

However, in analogous art, Schwarz discloses a method of inserting a pause within a BIST test algorithm implemented by the BISR circuit in Figure 1, as illustrated by the flow chart of Figure 6. At step 404, compare circuit 28 compares the state read from the cell with the expected state. At step 405, if there is an error, address re-map circuit 26 replaces the cell (or row containing the cell) with a redundant cell (or row). If the cell cannot be replaced, fail flag 44 is activated.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an address re-map circuit 26 as taught by Schwarz in the semiconductor device DUT of Ochi, for the purpose of repairing the DUT by replacing a defective cell (or row containing the defective cell) with a redundant cell (or row). A person skilled in the art would have been motivated to do so, since it is cost effective to repair expensive memory devices before disposal.

Regarding Claim 10, with respect to claimed fuse delete information, Ochi discloses an address re-mapping circuit 26, which receives the selected address from multiplexer 21 and, based on the address, re-maps the selected row to avoid faulty memory cells in memory array 12. Address re-map circuit 26 selectively drives redundant word lines 98 to avoid the faulty memory cells, as is known in the art.

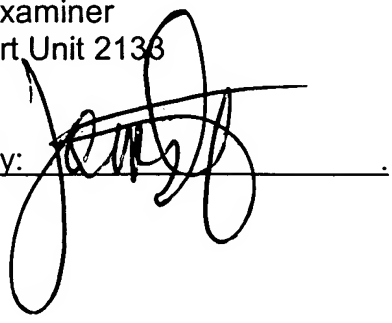
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: 

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Date: 1 September 2005
Office Action: Non-Final Rejection